In The United States Patent and Trademark Office

In re Application of: Kamalesh Srivastava, et al.	Filed: 05/31/2001
Application No.: 09/870,534	Examiner: Lynette T.Umez Eronini
For: A METHOD OF IMPROVING UNIFORMITY OF ETCHING OF A FILM ON AN ARTICLE	Art Unit: 1765
	Date: 11/21/2006

APPEAL BRIEF

Commissioner For Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

On even date herewith, Appellants appealed to the Board of Patent Appeals and Interferences from the decision of the Primary Examiner finally rejecting claims 1 to 12, 14 and 15. What follows is Appellants Appeal Brief as required by 37 CFR 41.47.

REAL PARTY IN INTEREST:

International Business Machines Corporation is the real party in interest in this appeal.

RELATED APPEALS AND INTERFERENCES:

There are no related appeals and interferences.

STATUS OF CLAIMS:

Claims 1 to 12, 14 and 15 are all of the claims pending in this appeal. Claim 13 was canceled without prejudice in Appellants' Amendment filed January 23, 2003. Claims 1 to 12, 14 and 15 are being appealed.

STATUS OF AMENDMENTS:

No amendment has been filed subsequent to the Final Rejection of August 24, 2006.

SUMMARY OF INVENTION:

In the semiconductor industry, so-called "solder bumps" are tiny quantities of solder used to connect semiconductor devices (also known as chips) and similar articles to chip packages and the like. Equivalent terms for solder bumps are C4, controlled collapse chip connection, solder balls, flip chip connection and C4 solder bump. The semiconductor devices and similar articles are usually made in rectangular arrays on a mono-crystalline slab of silicon, called a wafer. The solder bumps are placed on the semiconductor devices and similar articles while they are still joined in a wafer.

The solder bumps may be formed by the deposition of solder onto a continuous stack of metal films across the wafer to be bumped. The stack of metal films remains under the solder

bump in the final structure and forms the basis for the so-called ball limiting metallurgy, sometimes also called the underbump metallurgy. The stack of metal films is removed in between the solder bumps to electrically isolate them by suitable wet and/or dry electrolytic etching processes.

The challenge in the etching process is to effectively remove or etch the metal films without otherwise harming the solder bumps.

It has been found that wet etching of the stack of metal films is complicated by the presence of the solder bumps. The present inventors have further found that the stack of metal films wet etches slower at the kerf area of the semiconductor wafer where there are usually no solder bumps thereby making uniform etching of the semiconductor wafer difficult. Figure 1 of the present application illustrates a portion of a semiconductor wafer (i.e., one semiconductor device 30) having solder bumps 32, 34 and a kerf area 36. See also specification page 8, lines 1-15.

The present invention, then, is directed to a method of improving the uniformity of etching of metallic films having a plurality of solder bumps on semiconductor wafers. However, the teaching of the present invention can be applied also to the etching of nonmetallic films having a plurality of solder bumps on articles other than semiconductor wafers.

Figures 2 to 4 illustrate an apparatus for practicing the method of the present invention as embodied in independent claims 1 and 8. The semiconductor wafer/article 20 having a metallic or nonmetallic film and a plurality of solder bumps is mounted on rotating chuck 18 which is then immersed in a tank 24 of etchant 26. The semiconductor wafer 20 is rotated, continuously or sequentially as desired, for a predetermined amount of time so as to improve the uniformity of the etching of the film. The semiconductor wafer/article 20 is then removed from the tank 24 of etchant 26. (Specification page 10, lines 9-24 and page 11, line 1; claims 1 and 8).

It was found that the method of the present invention led to a marked improvement in the uniformity of the etching of the film. For example, one method of measurement of the uniformity of the etching of the film, the "wet etch uniformity", showed a 34% improvement in the wet etch uniformity according to the present invention. (Specification page 15, lines 1-9).

A copy of the claims on appeal are set forth in the Appendix.

GROUNDS OF REJECTION:

I. Whether claims 1, 4, 5 and 6 have been properly rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk U.S. Patent 5,340,437 in view of Datta et al. U.S. Patent 5,462,638.

I. Whether claims 2 and 3 have been properly rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk in view of Datta et al. and further in view of Takeshi et al. (English Abstract of JP 9115977 A2).

I. Whether claim 7 has been properly rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk in view of Datta et al. and further in view of Barbee et al. U.S. Patent 5,445,705.

I. Whether claims 8, 11, 12 and 14 have been properly rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk in view of Datta et al.

I. Whether claims 9 and 10 have been properly rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk in view of Datta et al. and further in view of Takeshi et al. (English Abstract of JP 9115977 A2).

I. Whether claim 15 has been properly rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk in view of Datta et al. and further in view of Barbee et al. U.S. Patent 5,445,705.

GROUPING OF CLAIMS:

All claims do not stand or fall together. Claims 1 and 8 stand together and claim 1 is representative of this group. Claims 2, 3, 9 and 10 stand together and claim 3 is representative of this group. The remaining claims will stand or fall based on the patentability of claims 1 and 8. Arguments for the separate patentability for these two groups of claims will be presented in the Argument section of this Appeal Brief.

ARGUMENT:

I. Claims 1, 4, 5 and 6 have been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk U.S. Patent 5,340,437 (hereafter "Erk") in view of Datta et al. U.S. Patent 5,462,638 (hereafter "Datta").

A. Patentability of Claim 1:

The Examiner has failed to state a prima facie case of obviousness with respect to claims 1, 4, 5 and 6.

The present invention as embodied in claim 1 is directed to the improved uniformity of etching of a film having a plurality of solder bumps. Appellants have found and asserted that this film etches slower at the kerf area of a semiconductor wafer where there are usually no C4 solder structures.(Appellants' specification page 3, lines 21-23 and page 4, line 1). Accordingly, in order to solve this problem first discovered by Appellants, Appellants have proposed rotating the wafer to improve the uniformity of etching. The combination of references proposed by the Examiner do not suggest the problem found by Appellants nor its solution. "[A] patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the 'subject matter as a whole' which should always be considered in determining the obviousness of an invention under 35 U.S.C. 103." In re Sponnable, 160 USPQ 237, 243 (CCPA 1969. The Examiner has not addressed this part of Appellants' invention in the Examiner's rejection of claim 1 and thus has failed to consider the "subject matter as a whole" of Appellants' invention.

Turning now to the references, Erk is directed to a process wherein a bare silicon wafer, which has been sawed and lapped, is immersed in an etchant bath and then rotated. The etching step is necessary to remove any work damage created by the sawing and lapping and to remove any embedded lapping grit. Among the objects of Erk are to uniformly etch the bare silicon wafer at slow rotation speeds and to have a relatively low total thickness variation across the wafer.

However, the Erk reference is distinguishable on at least three counts from Appellants' invention as embodied in claim 1. The first is that Erk is directed to the etching of bare silicon wafers to remove any residual effects of sawing and lapping. It is to be assumed that as a result of the etching process in Erk, such residual effects would be removed. There is nothing in Erk to

indicate that the teachings of Erk would be applicable to any other process other than the removal of such residual effects.

Second, Appellants' claim 1 is directed to a "method of improving the uniformity of etching of a film having a plurality of solder bumps" [emphasis added]. Improving the uniformity of etching is an important limitation of Appellants' claim 1. While Erk appears to address thickness variations, both locally and across the entire wafer (col. 2, lines 22-29), this is not the same as uniformly etching a film across the entire wafer as taught by Appellants. That is, Appellants want the same etching in the kerf area and the area with the solder bumps. Since Erk is etching a bare wafer, Erk cannot address this aspect of Appellants' invention.

Third, the teaching of Appellants' invention is that the presence of the solder bumps complicates the etching of the metal films (Appellants' specification page 3, lines 20-21). It cannot be assumed that the etching of a bare wafer as taught by Erk would be applicable to the etching of a wafer with a film having a plurality of solder bumps. Thus, there is no teaching in Erk to indicate that Erk would be applicable to improving the uniformity of etching of a film having a plurality of solder bumps as claimed by Appellants.

The deficiencies of Erk are not supplied by Datta. In the "Response to Arguments" section of the Final Office Action, the Examiner admits as much when the Examiner states that "Applicants' arguments, Erk's deficiencies and Datta's failure to cure Erk's deficiencies are acknowledged." (Final Office Action, page 9) [emphasis added] Datta is directed to the etching of one of the metallic films (i.e., TiW) underlying the solder bumps and merely teaches, as recognized by the Examiner, that for a semiconductor wafer having solder bumps, the metallic film is conventionally etched by dip etching. There is nothing in Datta to suggest the problem found by Appellants of nonuniform etching. Nor is there anything in Datta to suggest a method of etching by any other method than dip etching in a cassette-type etching process.

The Examiner concludes in the Office Action that "It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to employ any wafer, including a conventional wafer having solder bumps as disclosed by Datta in the process of Erk because Erk does not limit the specific types of wafers processed by the rotating etching process. It would appear that any wafer, including one with solder bumps, would benefit from the uniform etching process of Erk. Applicants have not shown anything unexpected by employing a conventional wafer with solder bumps in a known process for achieving uniform etching."

Appellants disagree with the Examiner's reasoning. As to the first sentence above, the Examiner states that it would have been obvious to combine Erk with Datta "because Erk does not limit the specific types of wafers processed by the rotating etching process." More correctly, since Erk is specifically and only directed to the etching of bare wafers to remove any work damage, there is no teaching in Erk that the process disclosed therein is useful for the etching of any other types of wafers. A "reference must be considered not only for what it expressly teaches, but also for what it fairly suggests." In re Burckel, 201 USPQ 67, 70 (CCPA 1979). Thus, the limits of what a reference teaches are what it expressly teaches or fairly suggests. Erk clearly does not expressly teach any wafers other than work-damaged wafers for processing by the rotating etching process. It is also submitted that there is no teaching in Erk to fairly suggest any other types of wafers for use in Erk's rotating etching process since Erk is directed to etching of wafers "to remove any work-damage created by the sawing and lapping and to remove any embedded lapping grit" (Erk specification, col. 1, ll 15-17) and there is no other teaching in Erk with respect to other wafers that may be used in Erk's rotating etching process.

As to the second sentence above, where is the teaching in Erk that "It would appear that any wafer...would benefit from the uniform etching process of Erk?" [emphasis added] It is submitted that the Examiner has substituted her opinion for any teaching found in Erk since Erk is specifically and only directed to the etching of bare wafers to remove any work damage.

As to the third sentence above, Appellants have shown unexpected results in their specification. Depending on the test methodology used, Appellants found improvement of 34% or 78% (page 15, Appellants' specification)! Assuming arguendo that the combination of Erk and Datta might result in some improvement in etching, the amount of the improvement found by Appellants is surprising and unexpected.

Any conceivable motivation provided by the Examiner above for the combining of Erk and Datta is negated by the fact that Erk and Datta use different processes and wafers in their respective etching processes. "The fact that a prior art reference can be modified to show the patented invention does not make the modification obvious unless the prior art reference suggests the desirability of the modification. An attempted modification of a prior art reference that is unwarranted by the disclosure of that reference is improper." In re Gordon, 221 U.S.P.Q. 1125, 1127 (CAFC 1984).

In the "Response to Arguments" section of the Final Office Action, the Examiner states that "the reason for combining Erk and Datta is that since Erk does not limit the specific types of wafers processed by the rotating etching process, then it would appear that any wafer, including one with solder bumps as taught by Datta, would benefit from the uniform etching process of Erk." (Final Office Action, page 10) However, Erk does in fact limit the specific types of wafers processed by the rotating etching process contrary to the Examiner's assertion. Erk is very specific to wafers that are work-damaged so as to remove the residual effects of sawing and lapping.

If modified as suggested by the Examiner above, there would be a different process than that claimed by Appellants since Erk and Datta do not use the same steps and film layer. That is, Erk has no film layer and no solder bumps and immerses and rotates the wafer in an etching bath.

Datta, conversely, does have a metallic film layer but etches the wafer in a cassette-type dip etching process. It should be readily apparent that Erk and Datta are directed to two different types of processes with two different kinds of wafers.

Given the flawed reasoning by the Examiner, it is submitted that the Examiner has yet to state a cogent motivation for combining Erk and Datta so as to render obvious Appellants' claim 1.

The Office has the burden under 35 USC §103 to establish a prima facie case of obviousness. In re Fine, 5 USPQ2d 1596 (CAFC 1597). "In determining whether a case of prima facie obviousness exists, it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modifications. [citations omitted] The prior art must provide one of ordinary skill in the art the motivation to make the proposed molecular modifications needed to arrive at the claimed compound."In re Lalu and Foulletier, 223 USPQ 1257, 1258 (CAFC 1984). "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 23 USPQ 2d 1780, 1783 (CAFC 1992).

In view of the preceding remarks, it is submitted that the Examiner has failed to state a prima facie case of obviousness with respect to claim 1. Accordingly, claim 1 should be allowable.

Inasmuch as claims 4 to 6 depend from claim 1, and claim 1 is believed to be allowable, then claims 4 to 6 should be allowable as well. No independent ground of patentability is asserted for claims 4 to 6.

II. Claims 2 and 3 have been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk in view of Datta and further in view of Takeshi et al. (English Abstract of JP 9115977 A2) (hereafter "Takeshi"). Claim 7 has been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk in view of Datta and further in view of Barbee et al. U.S. Patent 5,445,705 (hereafter "Barbee").

Inasmuch as claims 2, 3 and 7 depend from claim 1, and claim 1 is believed to be allowable, then claims 2, 3 and 7 should be allowable as well. No independent ground of patentability is asserted for claim 7.

A. Patentability of Claims 2 and 3:

Claims 2 and 3 are believed to be independently patentable.

The Examiner states that Erk in view of Datta fail to teach the step of sequentially rotating the article as claimed in claims 2 and 3. The Examiner further applies Takeshi which reads on rotating the article a predetermined amount but less than a complete rotation and repeating the step of rotating and etching. The Examiner concludes that it would have been obvious to modify Erk and Datta according to Takeshi "for the purpose of improving the method of detecting defects in semiconductor processing."

Erk and Datta have been discussed above. Takeshi discloses an analytical technique for detecting and analyzing so-called flow pattern defects (FPD) in semiconductor wafers. Takeshi is not directed at all to the problem faced by Appellants, to wit, improving the uniformity of a film having a plurality of solder bumps. The last statement above by the Examiner is telling. The Examiner has combined Erk, Datta and Takeshi "for the purpose of improving the method of

detecting defects in semiconductor processing." That is, the Examiner has combined Erk, Datta and Takeshi to teach a solution to a problem not faced by Appellants. It is submitted that Takeshi is nonanalogous art. "In order to rely on a reference as a basis for rejection of the applicant's invention, the reference must either be in the field of the applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." In re Oetiker, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992). "[T]he purposes of both the invention and the prior art are important in determining whether the reference is reasonably pertinent to the problem the invention attempts to solve. If a reference disclosure has the same purpose as the claimed invention, the reference relates to the same problem, and that fact supports use of that reference in an obviousness rejection. An inventor may well have been motivated to consider the reference when making his invention. If it is directed to a different purpose, the inventor would accordingly have had less motivation or occasion to consider it." In re Clay, 23 USPQ2d1058, 1061 (Fed. Cir. 1992). In the present case, the reference is directed to a different purpose, as admitted by the Examiner, and so should be considered to be nonanalogous art. Takeshi, then, should be withdrawn as a reference.

In the Final Office Action, the Examiner indicated that Erk, Datta and Takeshi may be combined "for the purpose of improving the method of detecting defects in semiconductor processing." (Final Office Action, page 5). Further, in the "Response to Arguments" section of the Final Office Action, the Examiner indicated that "Takeshi is analogous art because it is directed to a method of etching a wafer, which is immersed and rotated in an etchant and removed while observing the wafer for defects." (Final Office Action, page 11). Neither of these statements, however, pertain to Appellants' invention since Appellant is not interested in the defects as taught by Takeshi. Rather, Appellants are concerned with the uniformity of etching of a film having a plurality of solder bumps. That is, Appellants found that this film etches slower at the kerf area of a semiconductor wafer where there are usually no C4 solder structures. Thus,

since Appellants' invention is directed to a different purpose than Takeshi, it is submitted that Takeshi must be considered to be nonanalogous art.

Accordingly, with respect to claims 2 and 3, the Examiner has failed to state a prima facie case of obviousness.

III. Claims 8, 11, 12 and 14 have been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk in view of Datta et al.

The reasoning recited by Appellants for the allowability of claim 1 is equally applicable here for the allowability of claim 8. That reasoning recited earlier is incorporated by refererence herein. Accordingly, claim 8 should be allowable.

Inasmuch as claims 11, 12 and 14 depend from claim 8, and claim 8 is believed to be allowable, then claims 11, 12 and 14 should be allowable as well. No independent ground of patentability is asserted for claims 11, 12 and 14.

IV. Claims 9 and 10 have been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk in view of Datta et al. and further in view of Takeshi et al. (English Abstract of JP 9115977 A2). Claim 15 has been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Erk in view of Datta et al. and further in view of Barbee et al. U.S. Patent 5,445,705.

Inasmuch as claims 9, 10 and 15 depend from claim 8, and claim 8 is believed to be allowable, then claims 9, 10 and 15 should be allowable as well. No independent ground of patentability is asserted for claim 15.

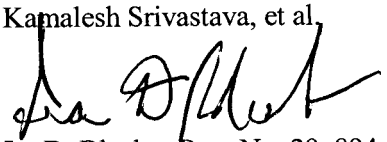
A. Patentability of Claims 9 and 10:

Claims 9 and 10 are submitted to be independently patentable for substantially the same reasons advanced in favor of claims 2 and 3 and those reasons are incorporated by reference herein.

SUMMARY:

For all the reasons presented, it is submitted that the Examiner's various decisions in rejecting Appellants' claims were in error and reversal of the Examiner's decisions is respectfully requested.

Respectfully submitted,
Kamalesh Srivastava, et al.



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CLAIMS APPENDIX

1. A method of improving the uniformity of etching of a film having a plurality of solder bumps on an article, the method comprising the steps of:

immersing the article containing the film having a plurality of solder bumps into a tank of etchant;

rotating the article while in the etchant for an amount of time so as to cause improved uniformity of etching of the film across the entire article compared to etching without rotating the article; and

removing the article from the tank of etchant.

2. The method of claim 1 wherein the step of rotating comprises sequentially rotating the article.

3. The method of claim 1 wherein the step of sequentially rotating comprises rotating the article an amount but less than a complete rotation, etching the article an amount of time, and repeating the steps of rotating and etching for an amount of time.

4. The method of claim 1 wherein the step of rotating comprises continuously rotating the article an amount of time.

5. The method of claim 1 wherein in the step of rotating, the article is rotated at a speed of 1 to 5 revolutions per minute.

6. The method of claim 1 wherein the film is a metallic film.

7. The method of claim 1 wherein the film is a nonmetallic film.

8. A method of improving the uniformity of etching of a film having a plurality of solder bumps on a semiconductor wafer, the method comprising the steps of:

immersing the semiconductor wafer containing the film having a plurality of solder bumps into a tank of etchant;

rotating the semiconductor wafer while in the etchant for an amount of time; and

removing the semiconductor wafer from the tank of etchant.

9. The method of claim 8 wherein the step of rotating comprises sequentially rotating the semiconductor wafer.

10. The method of claim 8 wherein the step of sequentially rotating comprises rotating the semiconductor wafer an amount but less than a complete rotation, etching the semiconductor wafer an amount of time, and repeating the steps of rotating and etching for an amount of time.

11. The method of claim 8 wherein the step of rotating comprises continuously rotating the semiconductor wafer an amount of time.

12. The method of claim 8 wherein in the step of rotating, the semiconductor wafer is rotated at a speed of 1 to 5 revolutions per minute.

14. The method of claim 8 wherein the film is a metallic film.

15. The method of claim 8 wherein the film is a nonmetallic film.

EVIDENCE APPENDIX

COPIES OF REFERENCES CITED BY THE EXAMINER TO FOLLOW

Erk et al. U.S. Patent 5,340,437

Datta et al. U.S. Patent 5,462,638

Barbee et al. U.S. Patent 5,445,705

Takeshi et al. JP 9115977A2

RELATED PROCEEDINGS APPENDIX

NO RELATED PROCEEDINGS